Class	Subclass

ISSUE CLASSIFICATION

PATENT NUMBER

1c09 09/751163 12/29/00

JC3/869

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED VR (3) Q.A. C	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/751163	D	257	400	2826 2823	K. Nguyen

APPLICANTS

Salvatore Storino
Andrew Davies

TITLE

Method for elimination of parasitic bipolar action in silicon on insulator (SOI) dynamic logic circuits

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip inside File Jacket

☒ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
☒ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. 6,271,086				ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ____months of this patent have been disclaimed.				ISSUE BATCH NUMBER	

(Assistant Examiner) (Date)

(Primary Examiner) (Date)

(Legal Instruments Examiner) (Date)

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